

Model Name: GA-B85M-D3H

SHEET	TITLE	Revision 1.11
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU_LGA1150-A	
05	CPU_LGA1150-B	
06	CPU_LGA1150-C	
07	DDR III CHANNEL A 1,2	
08	DDR III CHANNEL B 1,2	
09	PCH_FDI,DMI,USB,PCIE,NVRAM	
10	PCH_DP,CLK BUFFER	
11	PCH_HOST,SATA,PCI	
12	PCH_GPIO,CTRL,AUDIO	
13	PCH_PWR,GND	
14	PCI EXPRESS*16 SLOT	
15	PCI EXPRESS*4 SLOT	
16	PCI SLOT1,2	
17	ITE 8728 LPC IO	
18	COM,KB_MS_USB,USB30_20	
19	HWM,FAN CTRL,OV,-PROCHOT	
20	DUAL BIOS	
21	FP,FUSB,SPK,SATALED	
22	Realtek ALC892-GR	
23	REAR AUDIO JACK	
24	REALTEK RTL8111F	
25	DISCRETE POWER	
26	ATX , CLOCK GEN, TPM	
27	VCORE ISL95820_1	

SHEET	TITLE
28	VCORE ISL95820_2
29	RT8120_DDR POWER
30	LPT, M3 POWER
31	DVI, HDMI
32	IT8892E

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Model Name: GA-B85M-D3H

Component value change history

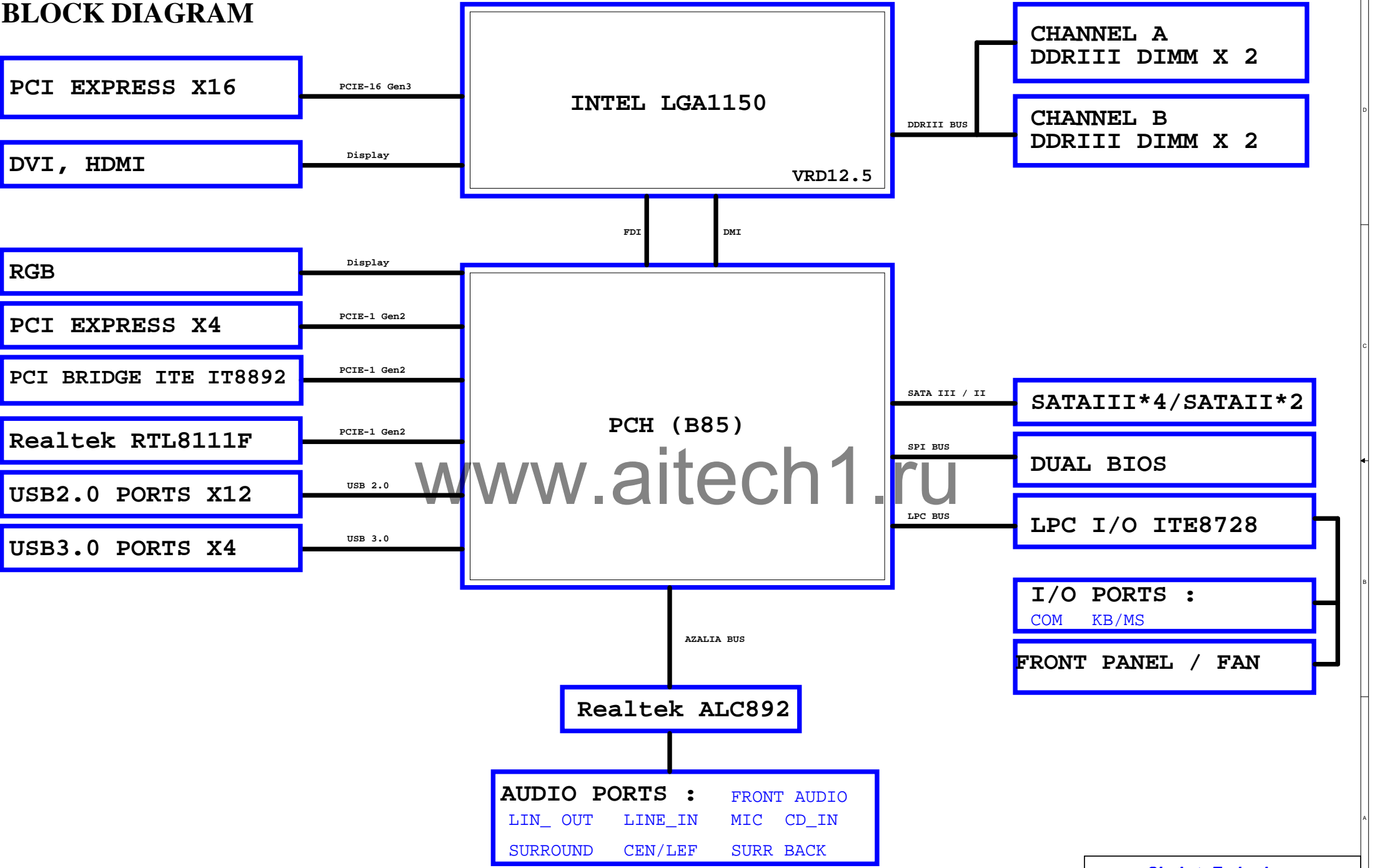
Revision 1.11
P-Code U12090-0

[illegible]

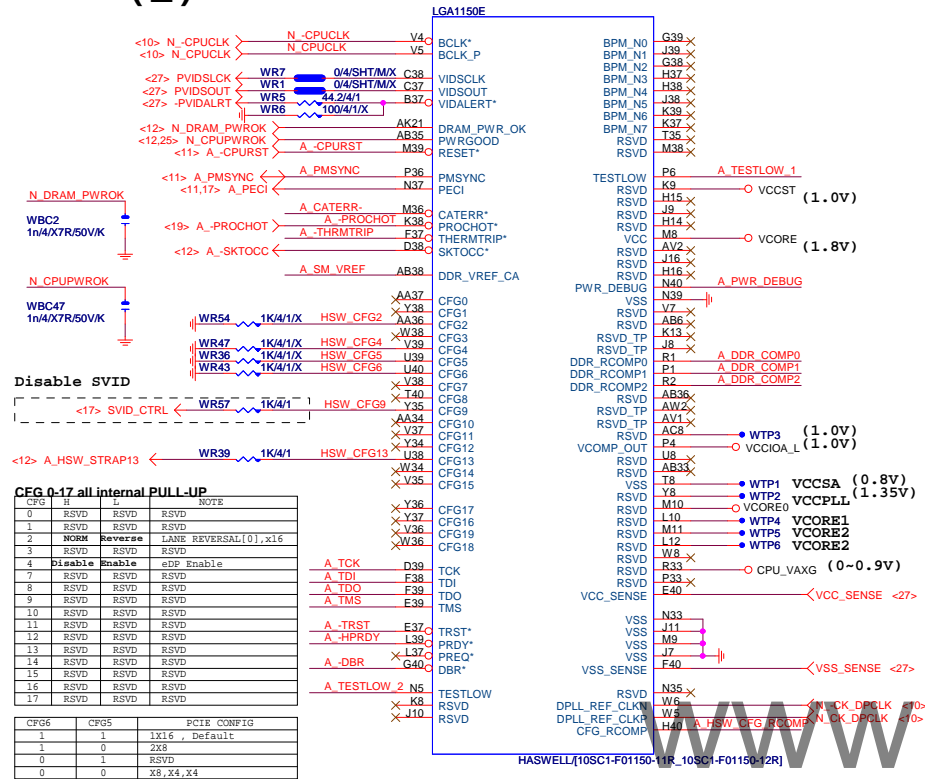
Circuit or PCB layout change

[illegible]

BLOCK DIAGRAM



LGA1150 (E)



HASWELL/10SC1-F01150-11R_10SC1-F01150-12R]

<8> VREF_DQB \	DDR_VREF_DQB
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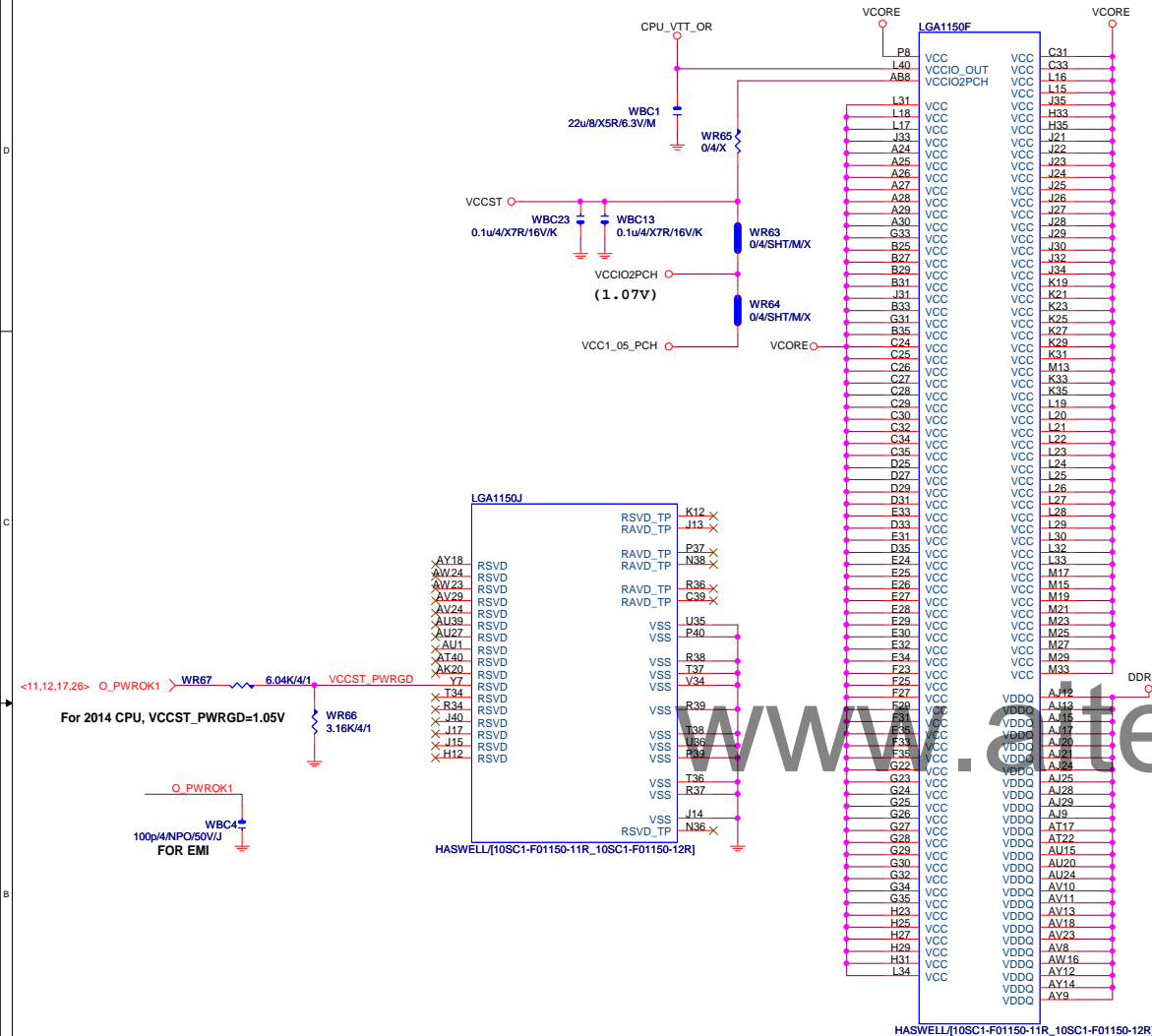


DDR BUS

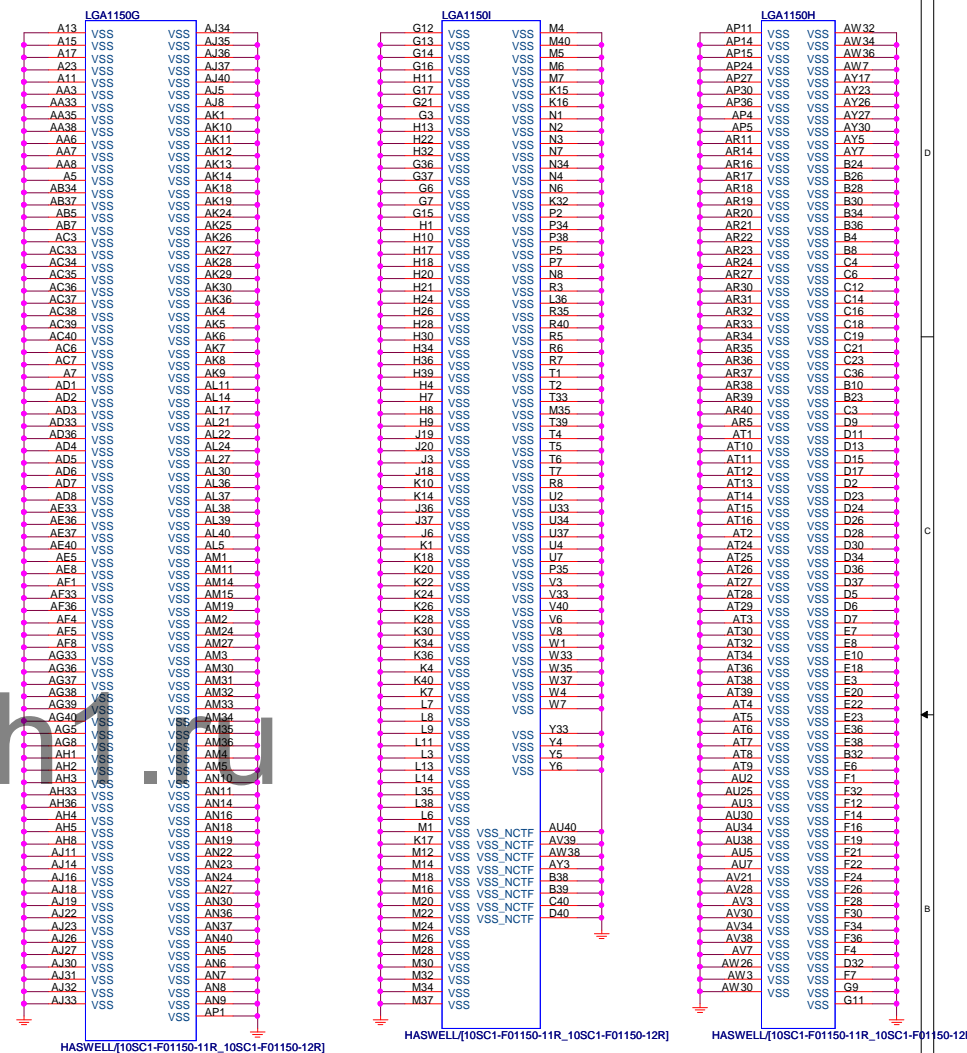
<7>	MODT_A[0..3]	↔	MODT_A[0..3]
<8>	MODT_B[0..3]	↔	MODT_B[0..3]
<7>	MDA[0..63]	↔	MDA[0..63]
<8>	MDB[0..63]	↔	MDB[0..63]
<7>	DQSA[0..7]	↔	DQSA[0..7]
<7>	-DQSA[0..7]	↔	-DQSA[0..7]
<7>	MAAA[0..15]	↔	MAAA[0..15]
<8>	MAAB[0..15]	↔	MAAB[0..15]
<8>	DQSB[0..7]	↔	DQSB[0..7]
<8>	-DQSB[0..7]	↔	-DQSB[0..7]

(F, J)

(1.0V)

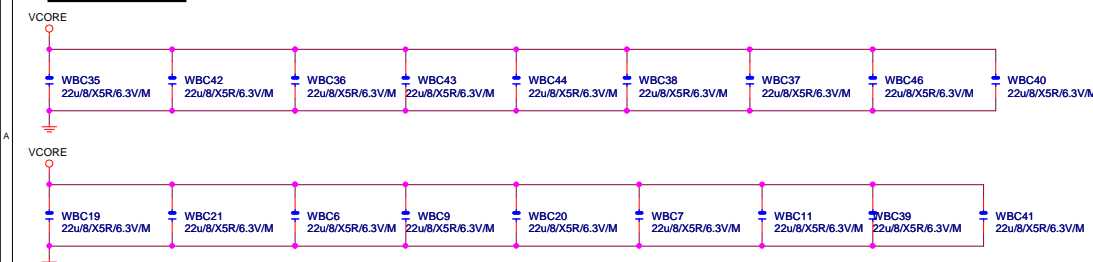


(G,H,I)



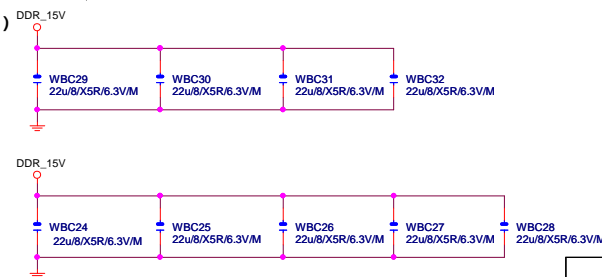
VCore CAP (X18)

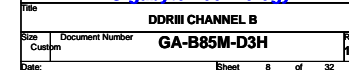
(X18)



DDR CAP (X9)

(x9)





PCH

(B)

DMI:12/4/4/4/12(breakout min 8/4/4/4/8)

Impedance=85 +- 17.5%

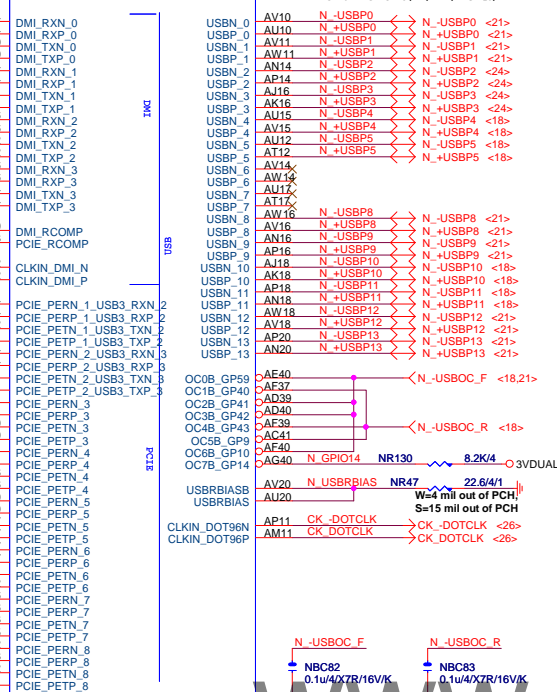
USB2.0 : 12/4.5/7.5/4.5/12 (breakout min 8/4/4/4/8)

Impedance=90 +- 17.5%

PCHB

B85: Port 6/7 N/A

H81: Port 6/7/12/13 N/A



放靠近 Device & PCI-E Slot

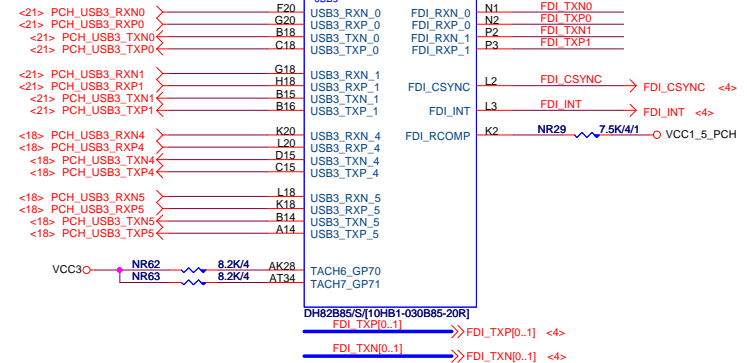
Impedance=80 +- 17.5%

PCIE1:16/5/5/5/16 (breakout min 8/4/4/4/8)

DH82B85/S[10HB1-030B85-20R]

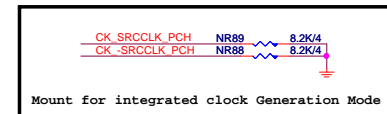
PCH

(F)

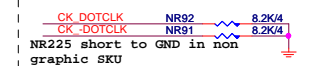


USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS
Impedance=85 +- 17.5%
Back Panel < 10000 MILS
Front Panel < 6000 MILS

PCH CLK PD



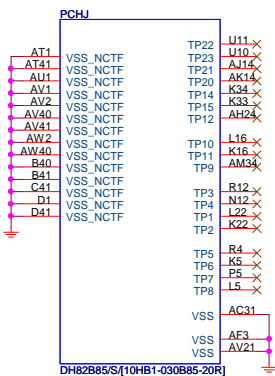
Mount for integrated clock Generation Mode



PCH

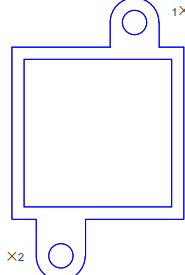
(J)

PCH H/S



DH82B85/S[10HB1-030B85-20R]

SB HEATSIN



PCH_HS
PCH_HS[12SP2-S04209-01R_12SP2-S04209-02R_12SP2-S04209-03R]

USB TABLE

OC[3:0]# for Device 29 (ports 0-7)

OC[7:4]# for Device 26 (ports 8-13)

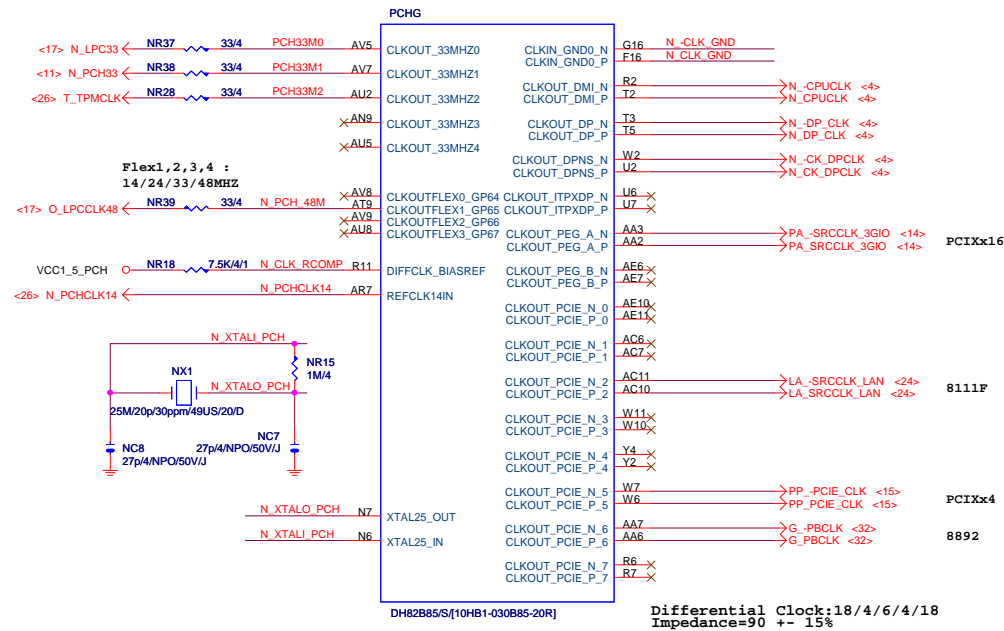
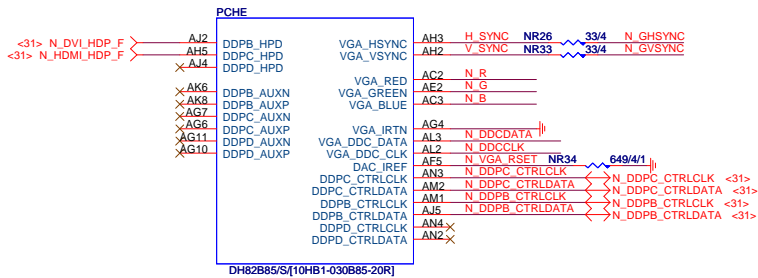
USB OC#	Configure
OC0#	F_USB30
OC1#	F_USB1
OC2#	F_USB2
OC3#	F_USB3
OC4#	USB_LAN
OC5#	R_USB30
OC6#	KB_MS_USB
OC7#	Not Use

Gigabyte Technology

Title			PCH FDI,DMI,USB ,PCIE,NVRAM	
Size	Document Number	GA-B85M-D3H		Rev 1.11
Custom				
Date:	Friday, September 13, 2013	Sheet	9	of 32

PCH (G)

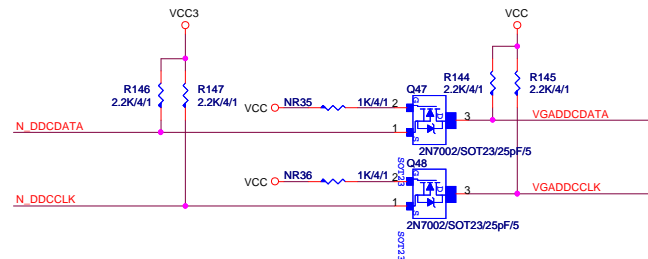
N -CLK_GND NR42 8.2K/4
N -CLK_GND NR41 8.2K/4



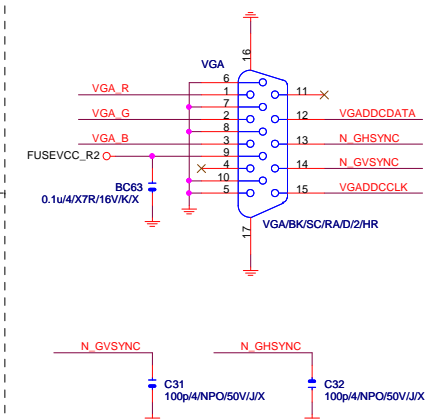
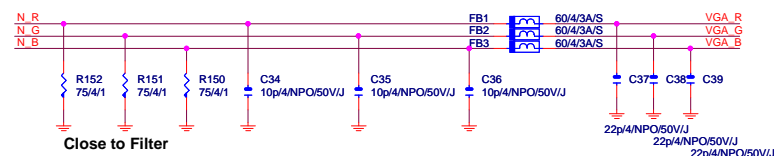
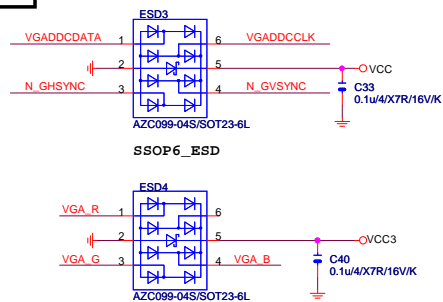
Differential Clock:18/4/6/4/18
Impedance=90 +- 15%

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VGA DDC



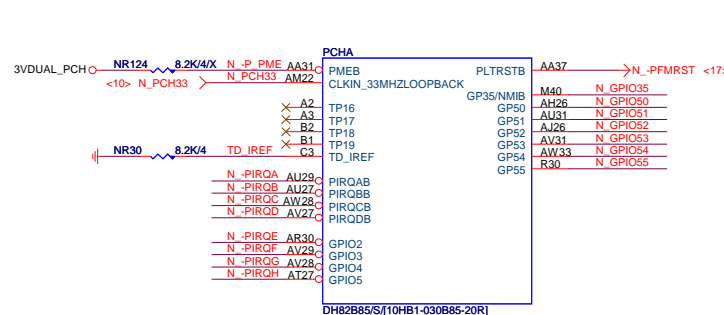
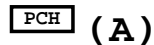
VGA DDC



Gigabyte Technology

Title			
PCH DISPLAY ,CLK BUFFER			
Size	Document Number	GA-B85M-D3H	Rev
Custom			1.11
Date:	Friday, September 13, 2013	Sheet	10 of 32

SATA3 : 20/7.5/4.5/7.5/20 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%
SATA2 : 15/7.5/4.5/7.5/15 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%



CK_SRCCLK SATA NR174 8.2K/4
CK -SRCCLK SATA NR173 8.2K/4

Mount for integrated Clock Generator Mode

[illegible]

H81 Port 2/3 N/A

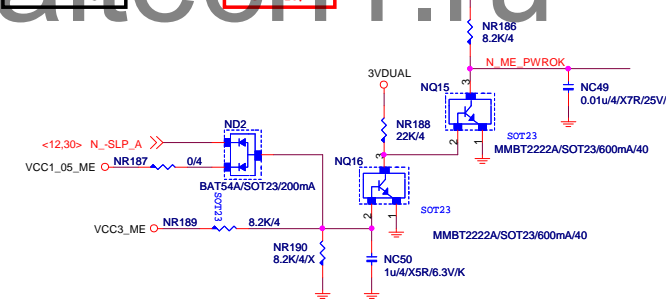
SATA3_2

SATA3_3

SATA2/7/WH/HOP/N/A/D/1/B/PA66

SATA2/7/WH/HOP/N/A/D/1/B/PA66

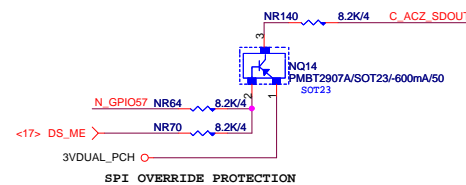
Z87 N/A



(D)



```
C_ACZ_SDOUT : HI --> ME Enable
              Lo --> ME Disable
HI:disable ME and override SOI Flash Access Permissions
```



At least 10ms delay after 3VDUAL_PCH stable

At least 40ns lead fall to 0V before 3VDUAL_PCH fall to 2V

The diagram illustrates the pinmux configuration for the N950 SoC, showing various peripheral connections and their pin configurations. The components are organized into several sections:

- Top Section:**
 - NR155:** 8.2K/4/X, N_GPIO45
 - NR139:** 8.2K/4/X, N_GPIO46
 - NR103:** 8.2K/4/X, N_GPIO47, N_GPIO57
 - NR106:** 1K/4/1, N_IGC_EN
 - NR153:** 1K/4/1/X, N_SUSCLK
 - NR105:** 8.2K/4/X
 - NR154:** 8.2K/4/X
- Left Section:**
 - GP8:Low to enable PCH clock chip
 - SUSCLK:Low to OD PLL VR
 - GP28:Lo disable VRM ,Hi enable VRM
- Right Section:**
 - NRN9:** 8.2K/8P4R/4
 - NRN10:** 8.2K/8P4R/4
- Bottom Section:**
 - NR145:** 8.2K/4/X, N_GPIO20, N_GPIO1, N_SYS_RST
 - NR48:** 8.2K/4/X, N_GPIO33
 - NR109:** 1K/4/1
 - NR115:** 8.2K/4
 - NR162:** 8.2K/4/X
 - NR49:** 8.2K/4
- Bottom Right Section:**
 - N_S_WARN:** NR129, 8.2K/4
 - N_GPIO27:** NR60, 8.2K/4
 - N_GPIO31:** NR72, 8.2K/4
 - N_SLP_LAN:** NR73, 2K/4/X
 - N_GPIO72:** NR100, 8.2K/4
 - N_PCIE_WAKE:** NR76, 1K/4/1
 - N_GPIO29:** NR95, 1K/4/1/X
- Bottom Left Section:**
 - N_PCH_RST:** NR172, 20K/4/1
 - N_PCH_TDI:** NR170, 200/4/1
 - N_PCH_TDO:** NR141, 200/4/1
 - N_PCH_TMS:** NR169, 200/4/1
 - N_PCH_TCK:** NR87, 200/4/1/X
- Bottom Center Section:**
 - N_PCH_RST:** NR143, 1K/4/1/X
 - N_PCH_TDI:** NR171, 100/4/1
 - N_PCH_TDO:** NR168, 100/4/1
 - N_PCH_TMS:** NR142, 100/4/1
 - N_PCH_TCK:** NR108, 514/1
 - N_GPIO18:** NR79, 8.2K/4
 - N_GPIO73:** NR134, 8.2K/4
 - N_GPIO26:** NR107, 8.2K/4
 - N_GPIO25:** NR137, 8.2K/4
 - N_SYS_RST:** NC59, 1n4/X/2R/50V/K
 - N_DRAM_PWROK:** NC59, 1n4/X/2R/50V/K

The diagram uses color coding to distinguish between different types of connections: blue for NR155, NR139, NR103, NR106, NR153, NR145, NR48; red for NR105, NR154, NR109, NR115, NR162, NR49, NR129, NR60, NR72, NR73, NR100, NR76, NR95, NR172, NR170, NR141, NR169, NR87, NR143, NR171, NR168, NR142, NR108, NR79, NR134, NR107, NR137, NC59; and green for NRN9, NRN10, NR129, NR60, NR72, NR73, NR100, NR76, NR95, NR172, NR170, NR141, NR169, NR87, NR143, NR171, NR168, NR142, NR108, NR79, NR134, NR107, NR137, NC59.

NX2-SHT
SHW/D0.64*5.08*6.74

N Y1
N Y2

NR75 10M/4 NX2

32.768K/12.5p20ppm/TFS38/35K/4

NC16 NC18
18P4/NPO/50V/J 18P4/NPO/50V/J

CLR_CMOS

BATTERY CR2032

ND1
BAS40-05/0.2A/SOT23

NR340 06/SHT/M/X

NR340 06/SHT/M/X

NR67 390K/4

NR78 20K/4/1

NC15 1u4/X5R/6.3V/K

NC20 1u4/X5R/6.3V/K

CLR_CMOS

N_RTCVDD <13,19>

N_INTRVDD <13,19>

N_RTCRST

PH1*2BK/2.54/VA/D

BATTERY-DUAL-4

RB 必須放在BAT外

N_INTRUDER NR74 1M/4

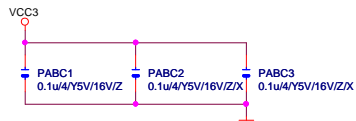
N_SRTCST NR77 20K/4/1

NC19 1u4/X5R/6.3V/K

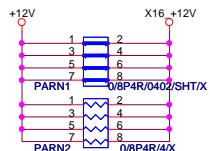
VCC3 PENC1 0.1u4/Y5V16V/Z

Title			
PCH GPIO , CTRL , AUDIO			
Size	Document Number		Rev
Custom	GA-B85M-D3H		1.1
Date:	Friday, September 13, 2013	Sheet	12 of 32

PCIEX16 CAP



PCIEX16 PROTECT SHT

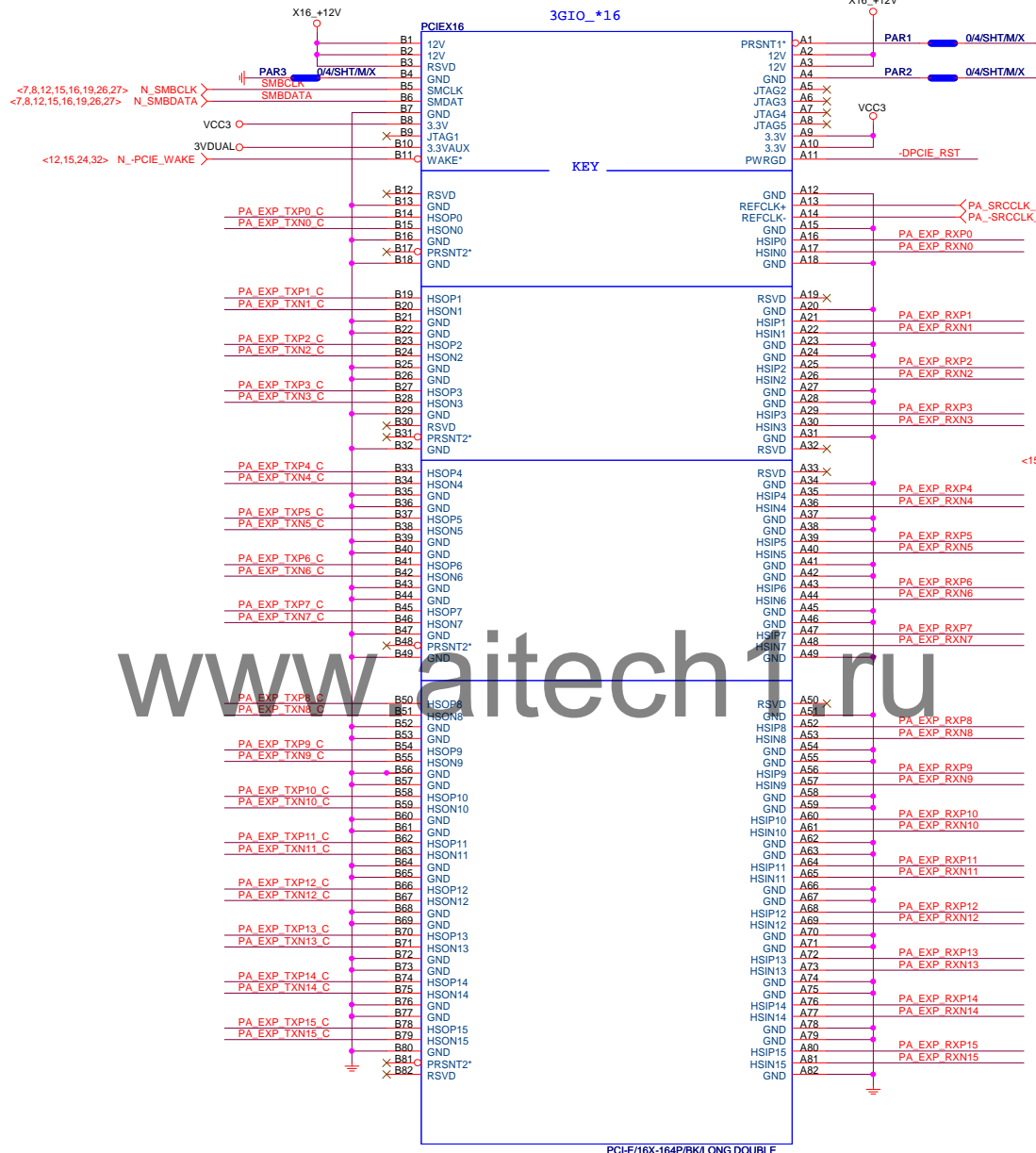


PCIEX16 AC CAP

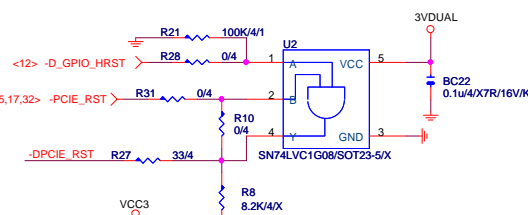
PA EXP TXP0	PAC5	0.22u4/X5R6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u4/X5R6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u4/X5R6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R6.3V/K	PA EXP TXN15 C

PA EXP RXP[0..15] >>> PA_EXP_RXP[0..15] <4>
 PA EXP RXN[0..15] >>> PA_EXP_RXN[0..15] <4>
 PA EXP TXP[0..15] >>> PA_EXP_TXP[0..15] <4>
 PA EXP TXN[0..15] >>> PA_EXP_TXN[0..15] <4>

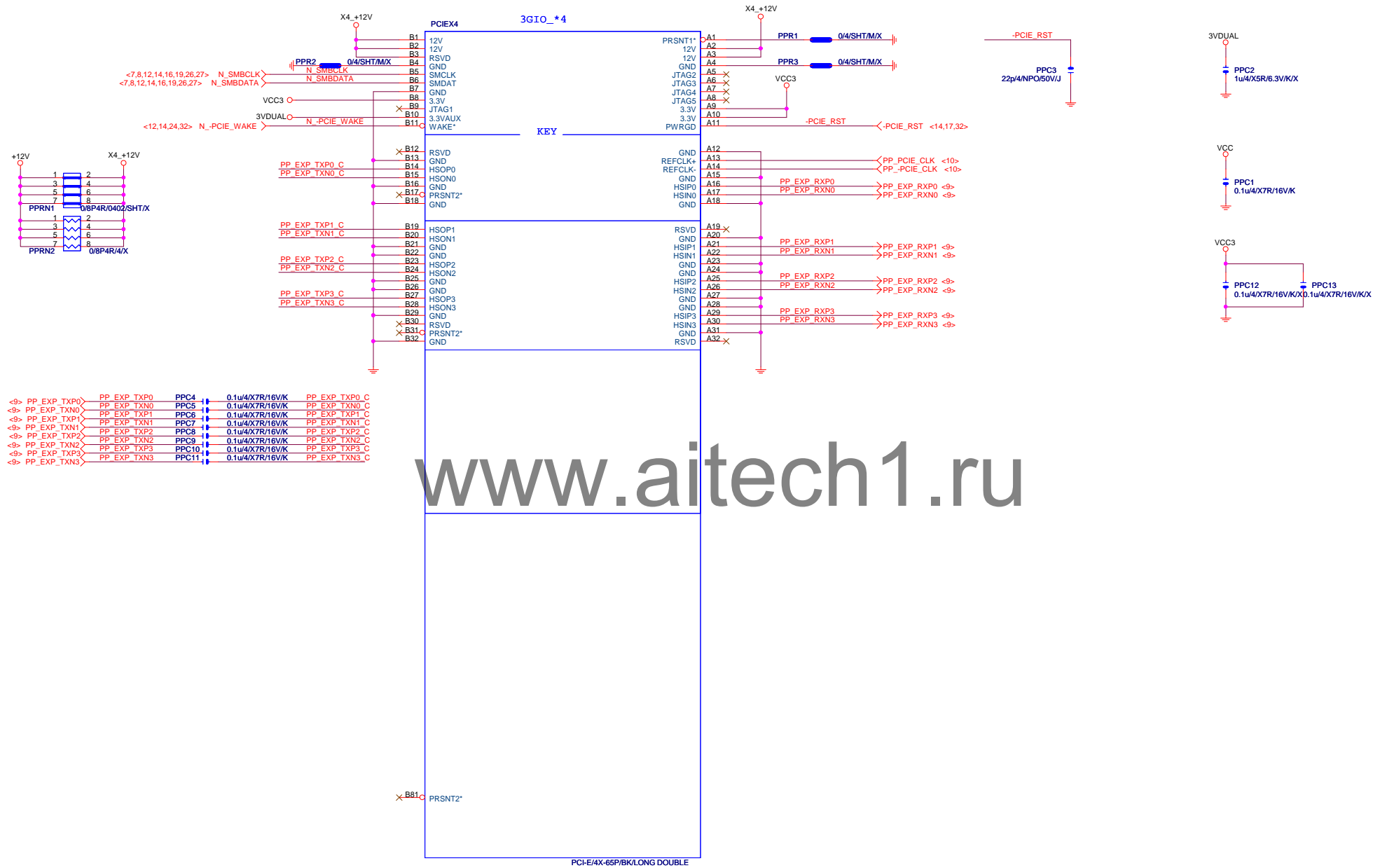
PCIEX16 SLOT



The auxiliary reset circuit is only required for PCIe Gen3 margining and functional link training



PCIEX4 SLOT

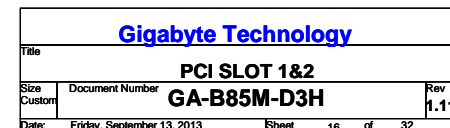


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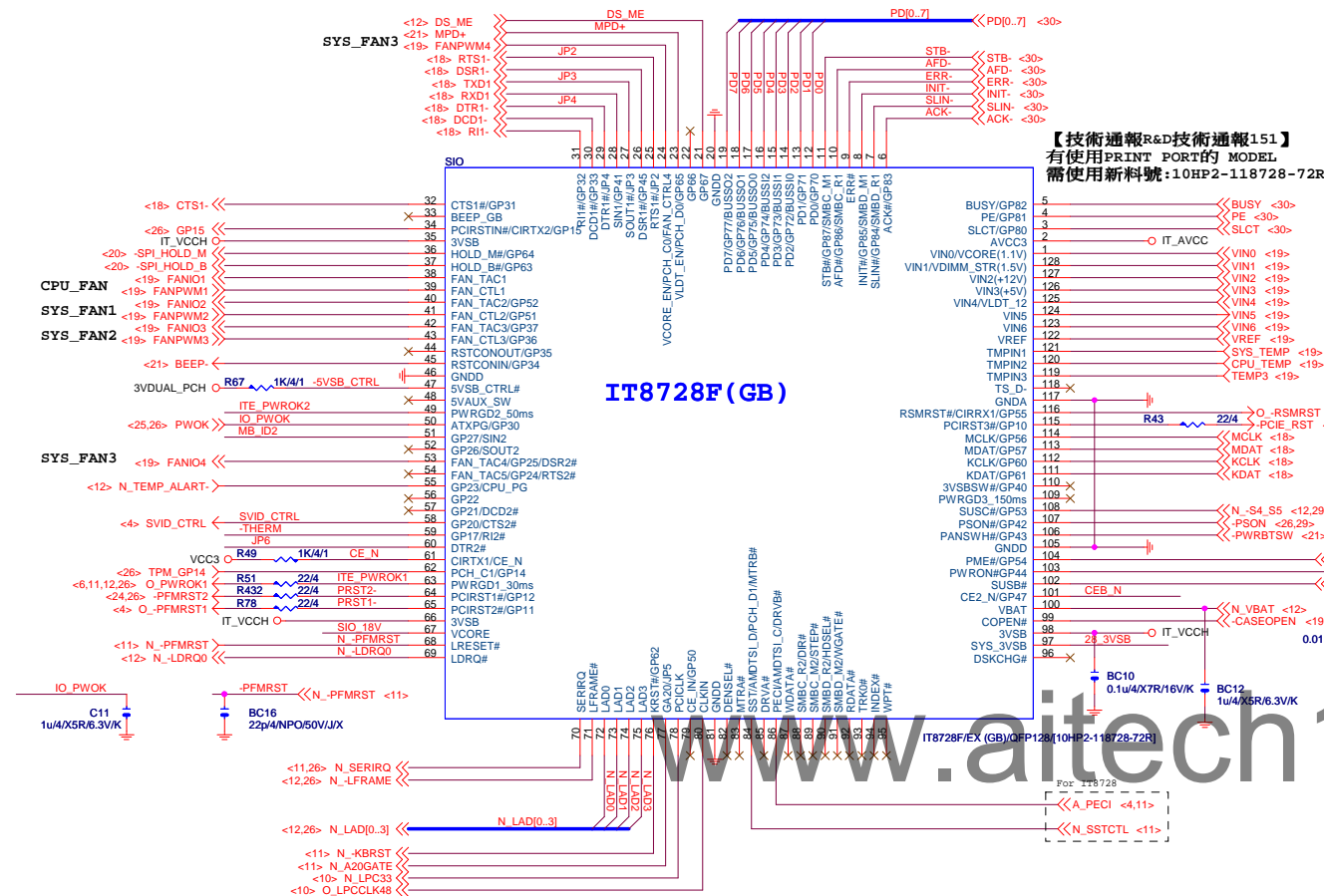
PCI SLOT 2	
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PCI CAP



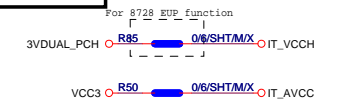
SIO IT8728F



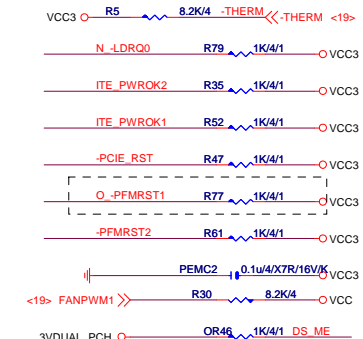
IT8728F (GB)

【技術通報R&D技術通報151】
有使用PRINT PORTの MODEL
需使用新料號:10HP2-118728-72R

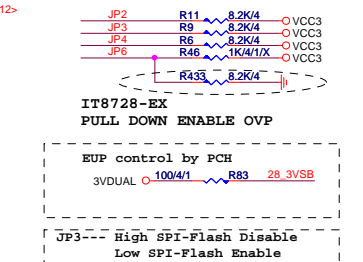
PWR SHT



SIO PU



SIO STRAP



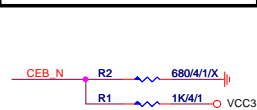
MB ID



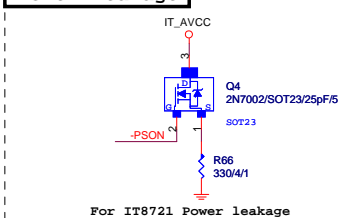
IT8728F NOTE

	IT8728
PIN121	VCORE_EN/PCH_C0
PIN120	VLDT_EN/PCH_D0
PIN19	ATXPG
PIN31	PCH_C1
PIN53	SST/AMDTSLI_D/MTRB# /PCH_D1
PIN55	PECI/AMDTSLI_C/DRV#
PIN66	SYS_3VSB
PIN70	GP47
PIN95	VIN2(VCC5)
PIN96	VIN1(VCC12)
PIN97	VIN1/VDIMM_STR(1.5V)
PIN98	VIN0/VCORE(1.1V)/NC

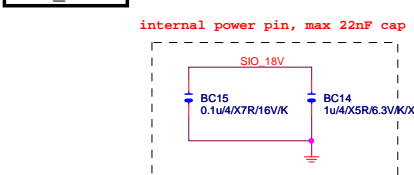
DUAL BIOS OPT STRAP



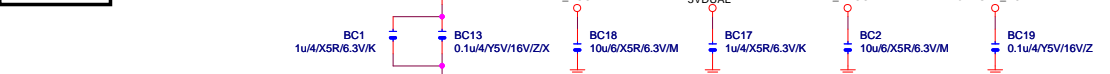
Power leakage



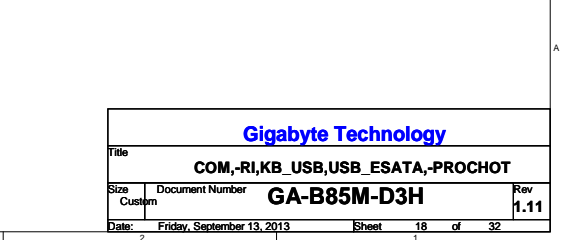
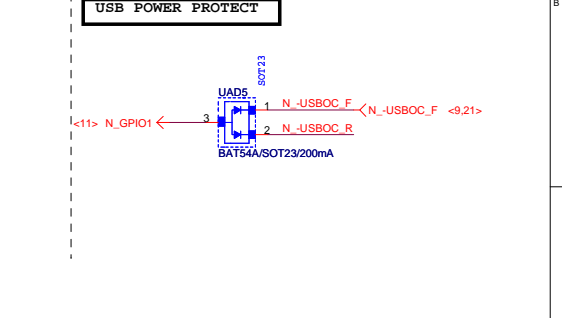
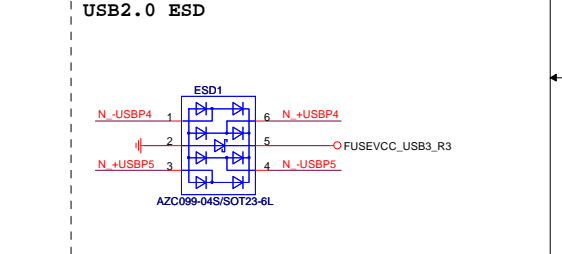
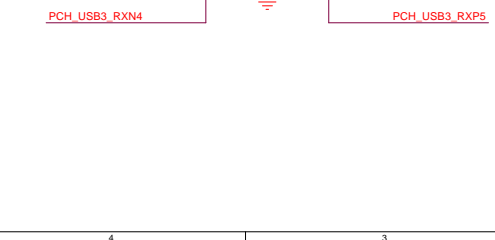
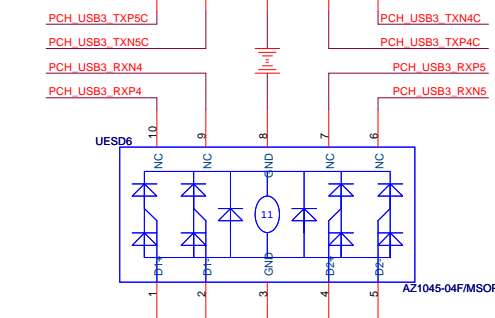
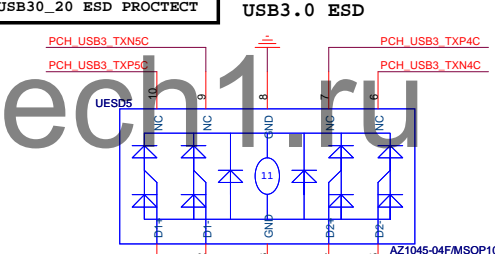
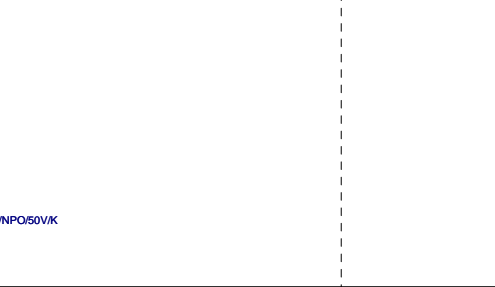
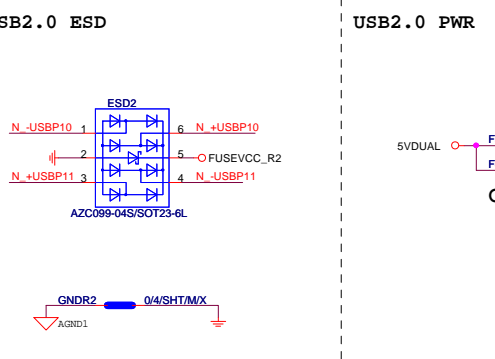
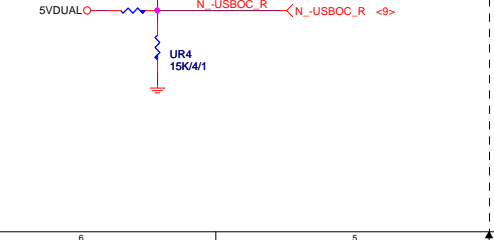
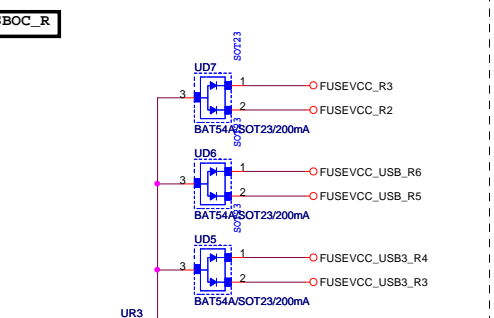
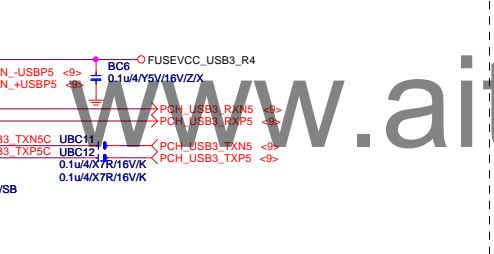
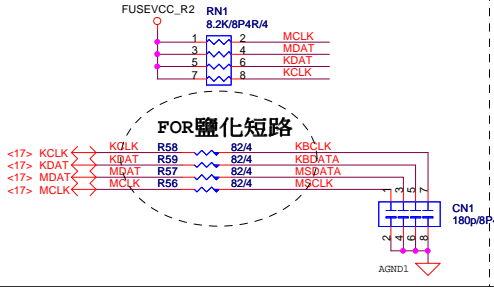
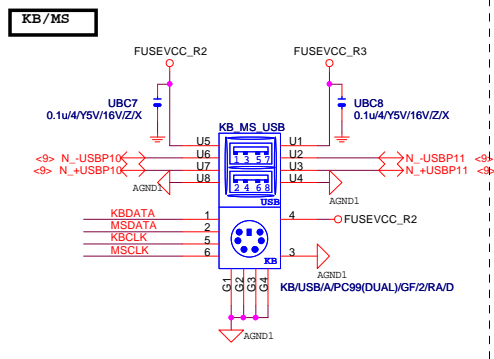
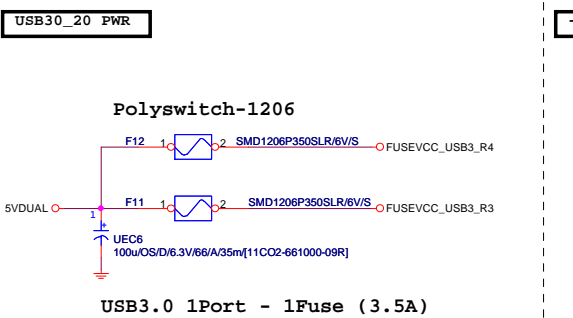
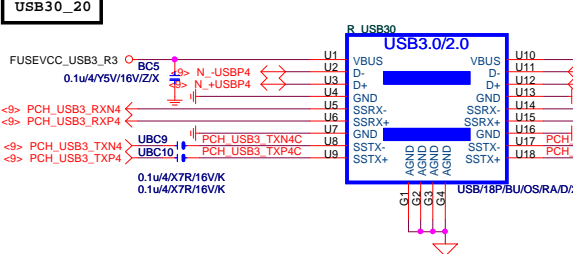
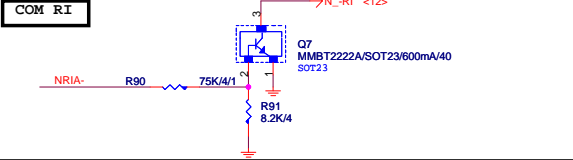
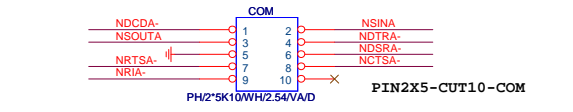
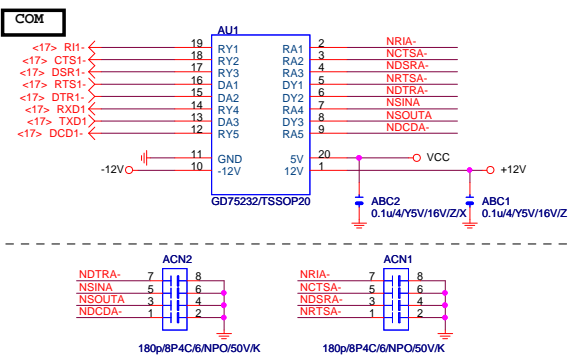
SIO_18V

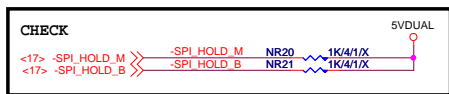
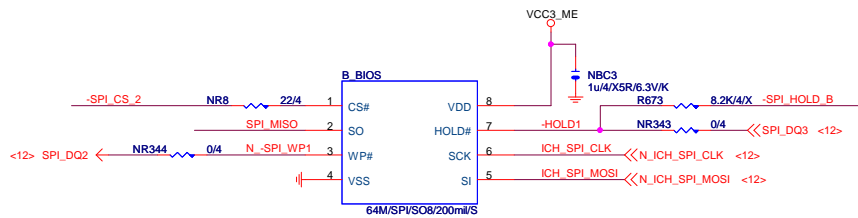
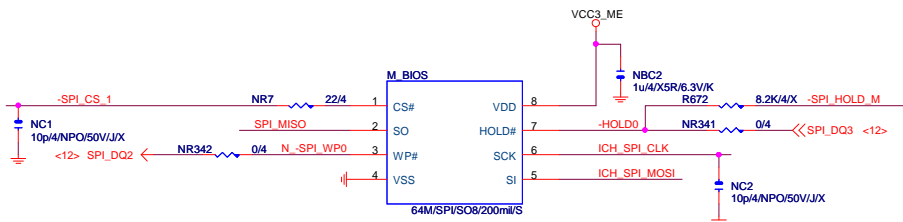


SIO CAP

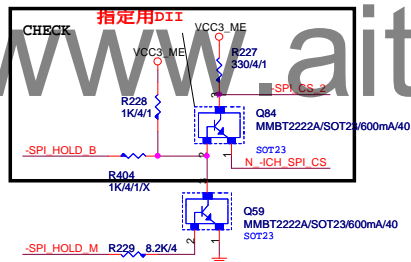
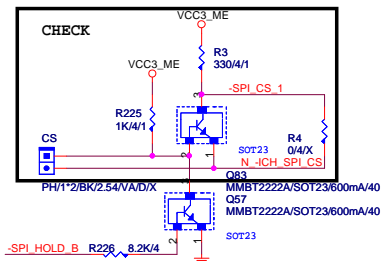


Gigabyte Technology			
Title	ITE 8728 LPC IO		
Size	Document Number	GA-B85M-D3H	Rev 1.11
Date:	Friday, September 13, 2013	Sheet 17	of 32



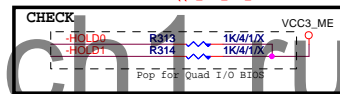
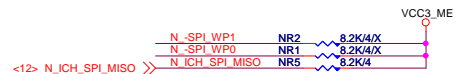
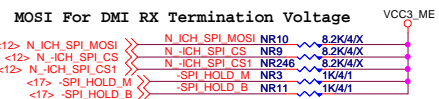


Dual BIOS CS connect
circuit update



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

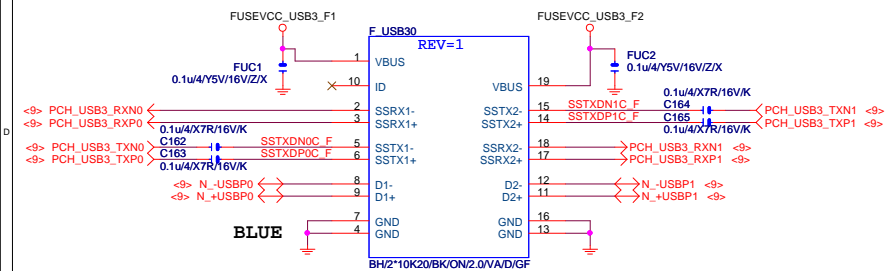
1 means floating
0 means PD 1k



Gigabyte Technology

Title		
DUAL BIOS		
Size	Document Number	Rev
Custom	GA-B85M-D3H	1.11
Date:	Friday, September 13, 2013	Sheet 20 of 32

F_USB30



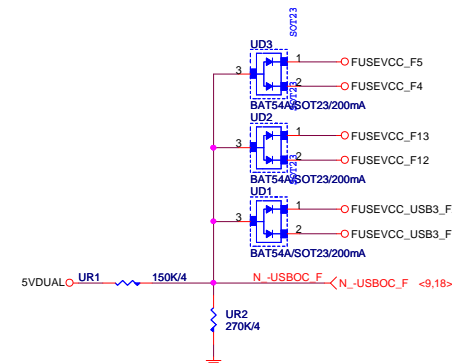
F_USB30 PWR

Polyswitch-1206

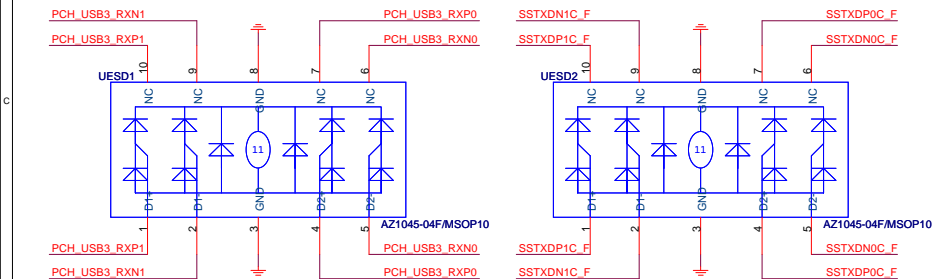


USB3.0 1Port - 1Fuse (3.5A)

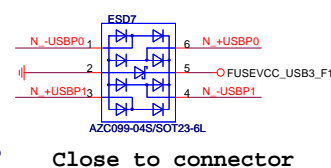
-USB0C_F



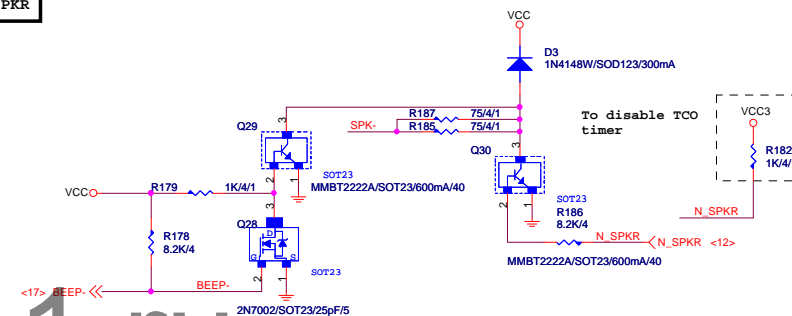
F_USB30 ESD PROTECT



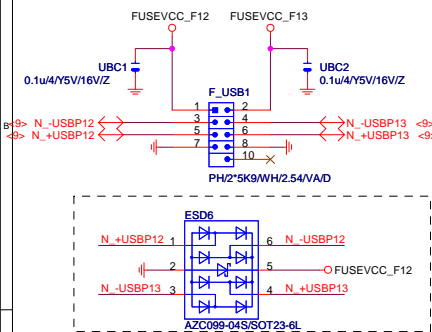
SPKR



Close to connector

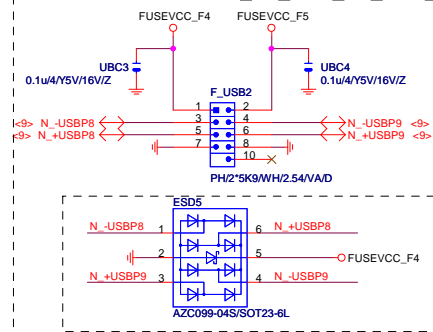


FRONT USB1



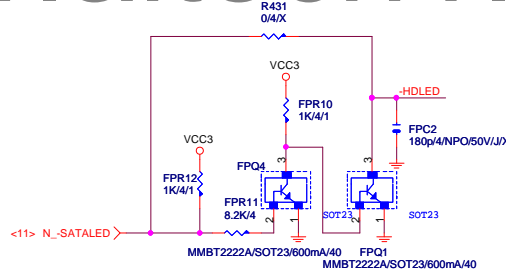
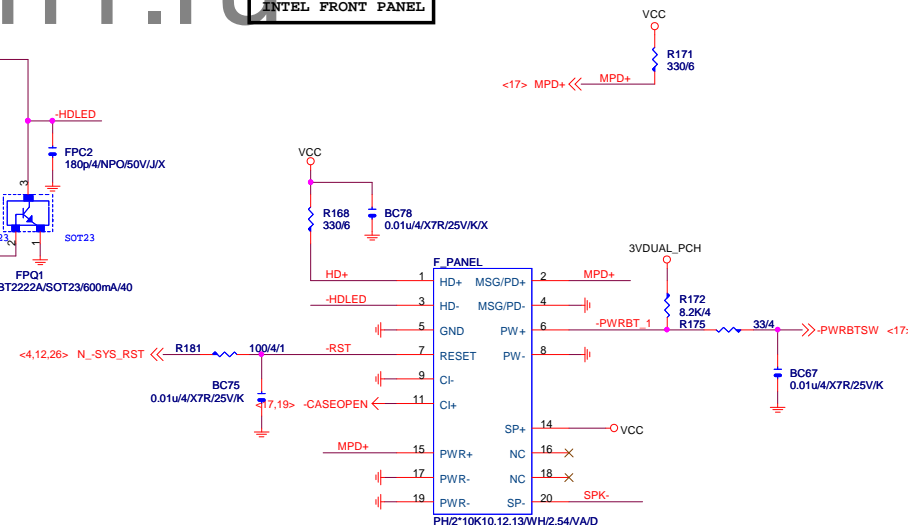
Close to connector

FRONT USB2



Close to connector

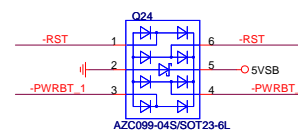
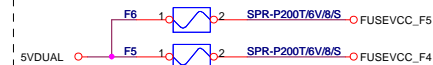
SATA LED

[illegible]

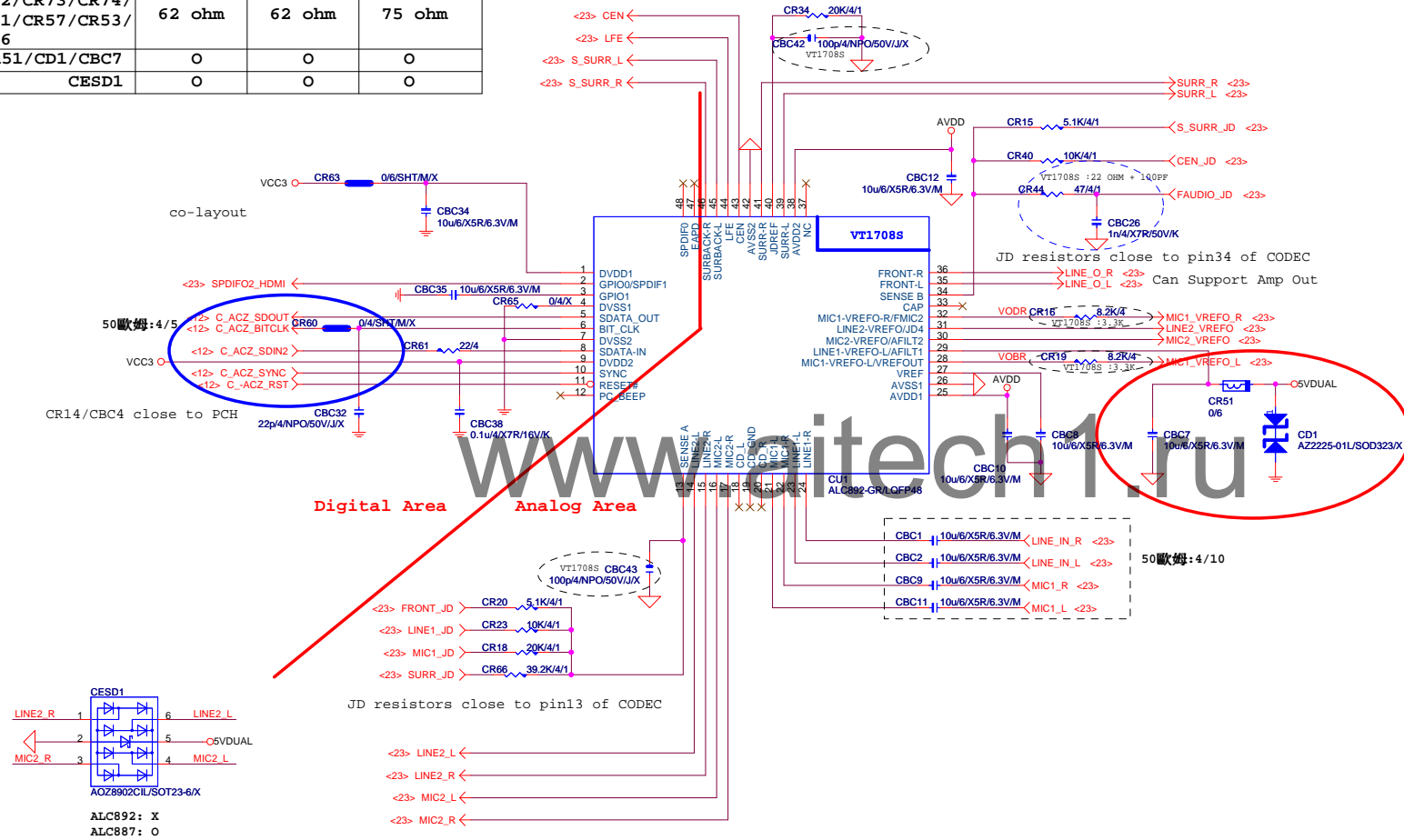
FUSE-0805

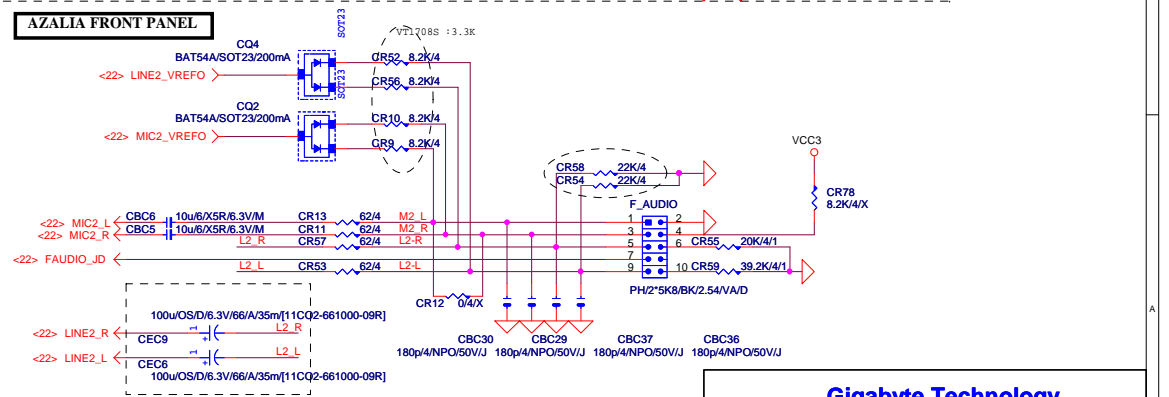
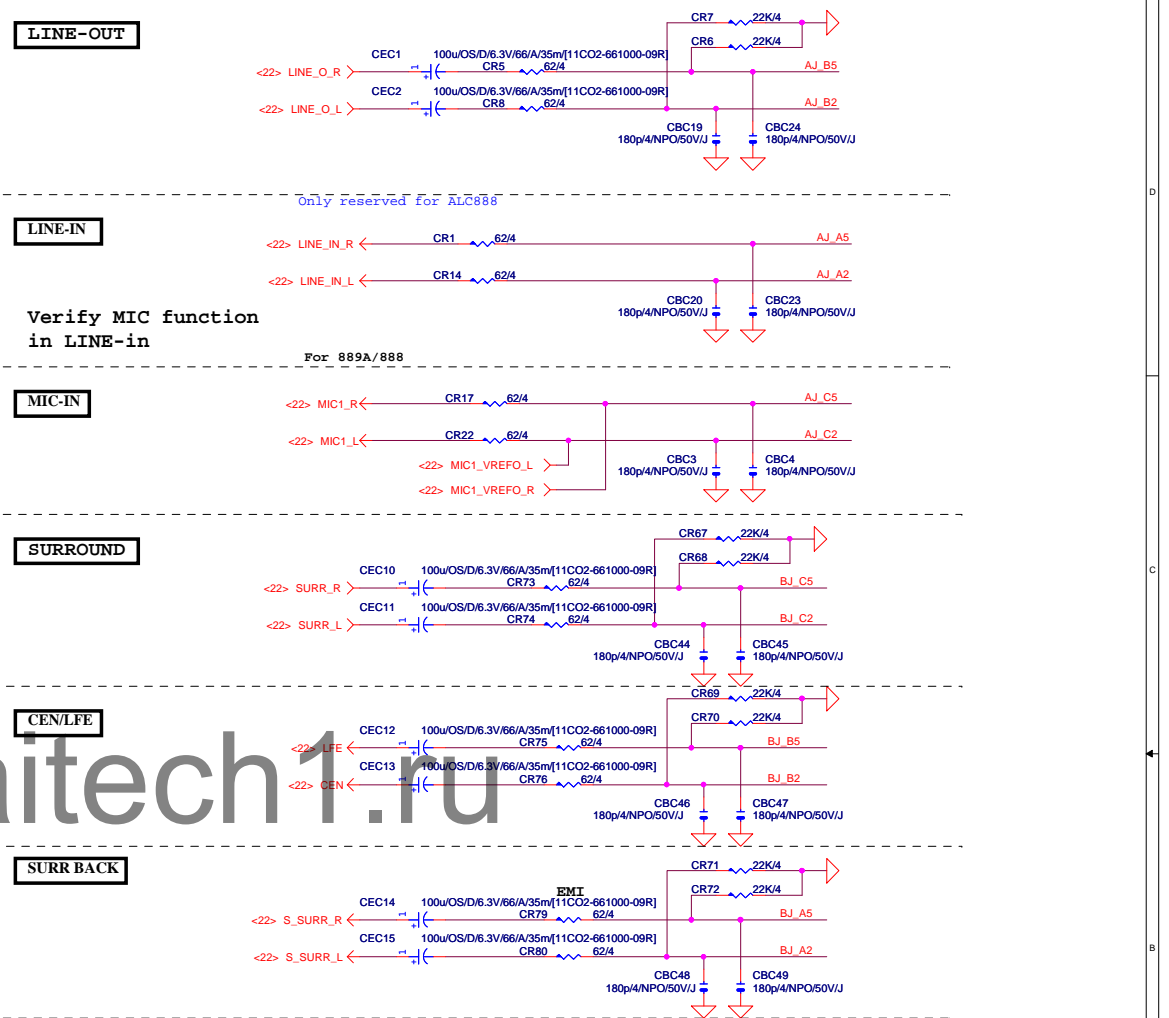
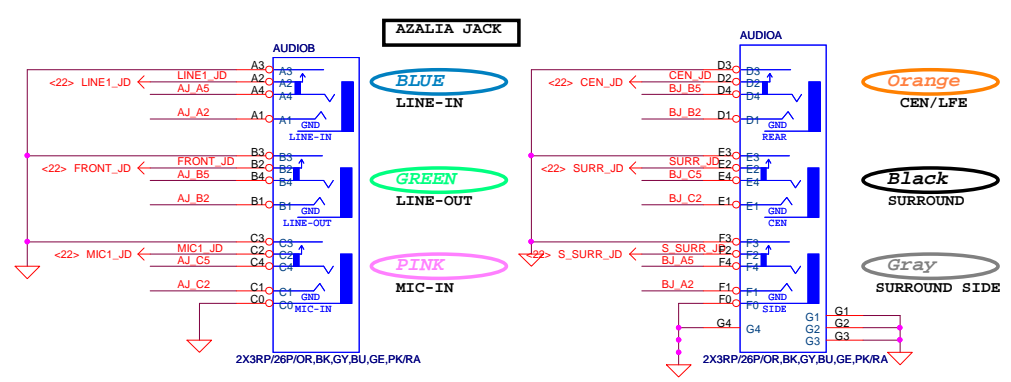
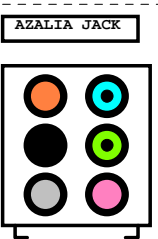
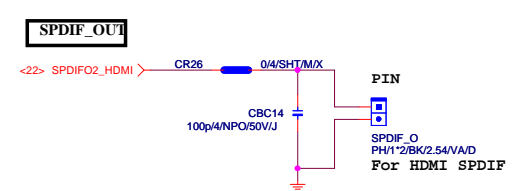
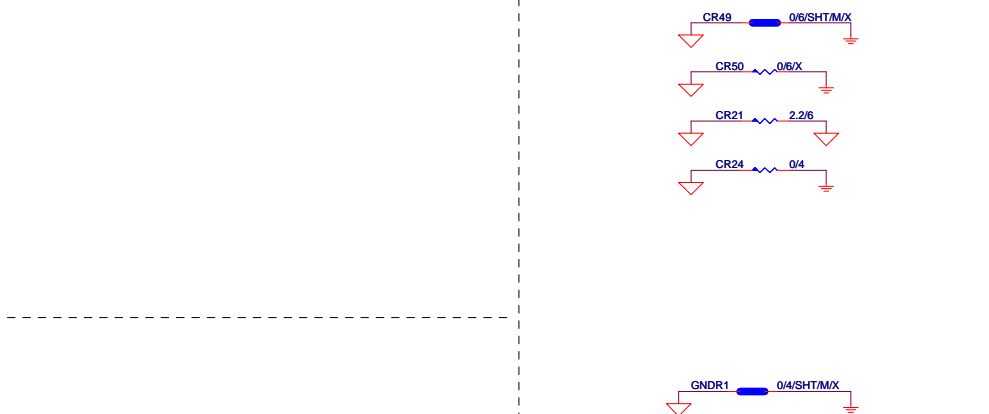


FUSE-0805



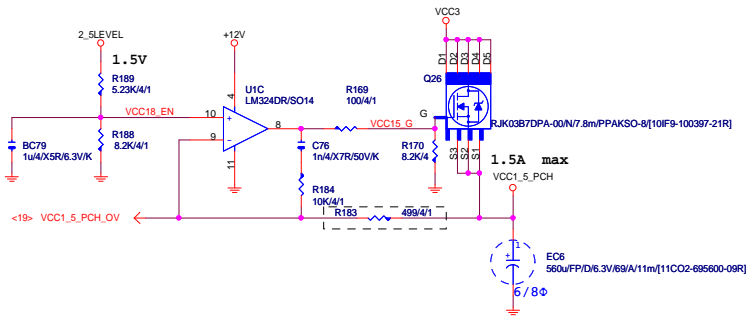
	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	O	O	O



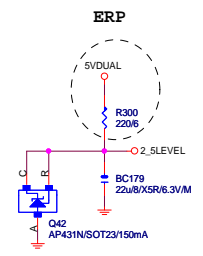


Gigabyte Technology			
AUDIO JACK			
GA-B85M-D3H			
Title	Document Number	Rev	1.11
Size Custom			
Date: Friday, September 13, 2013	Sheet	23	of 32

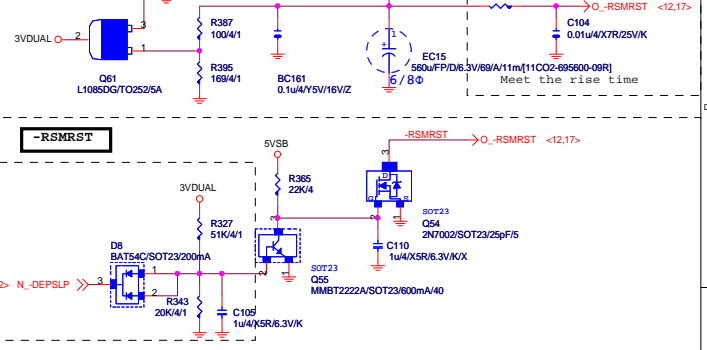
VCC1_8_PCH



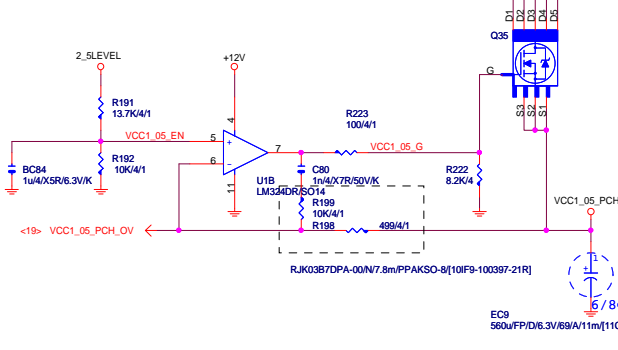
2_5LEVEL



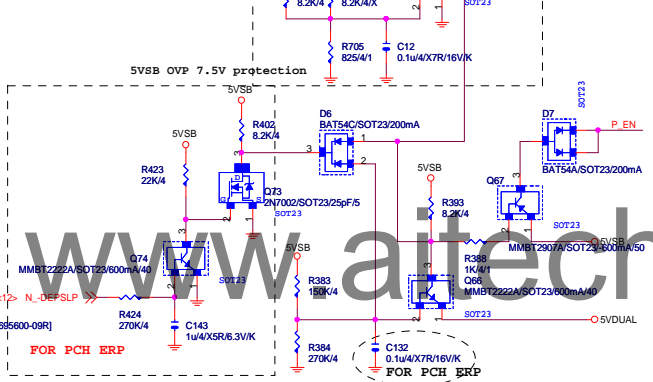
3VDUAL



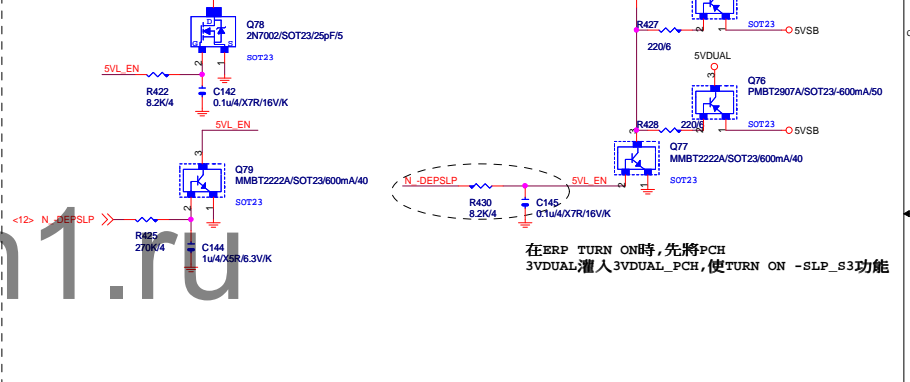
VCC1_05_PCH



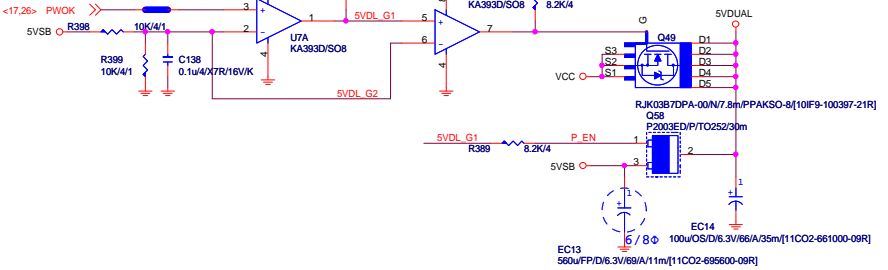
5VDUAL SHORT PROTECT



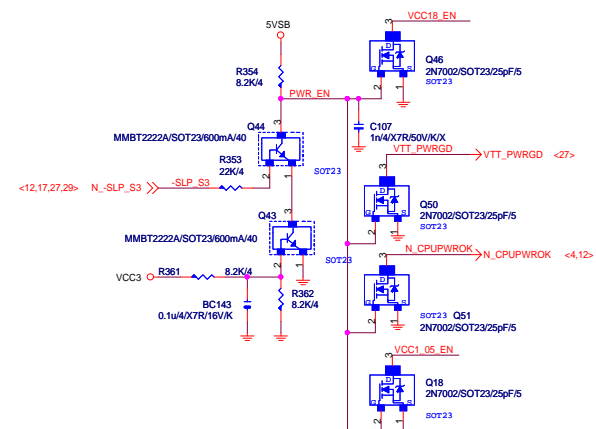
PCH ERP



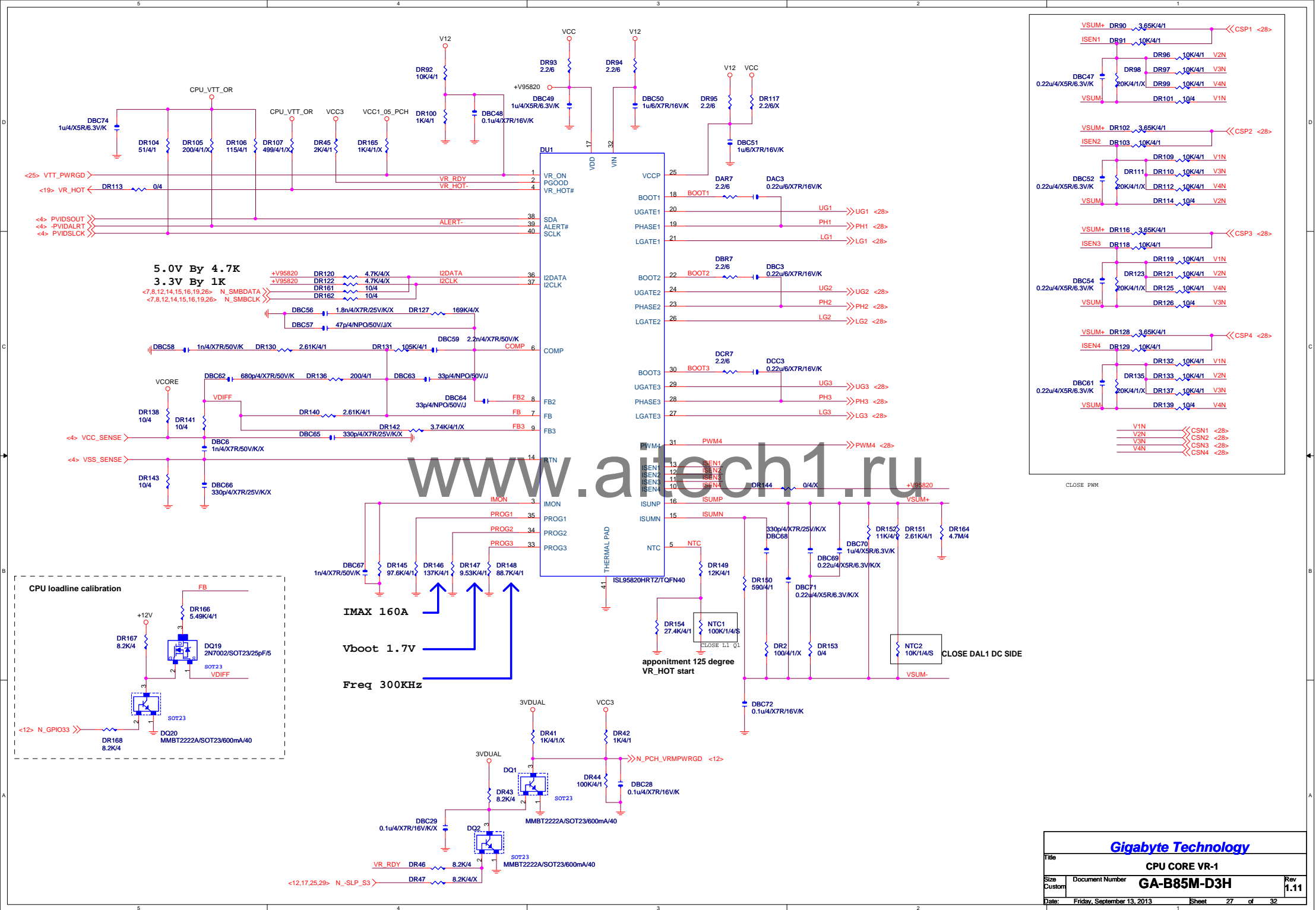
5VDUAL

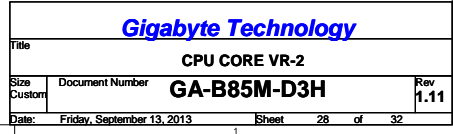


PWR SEQ

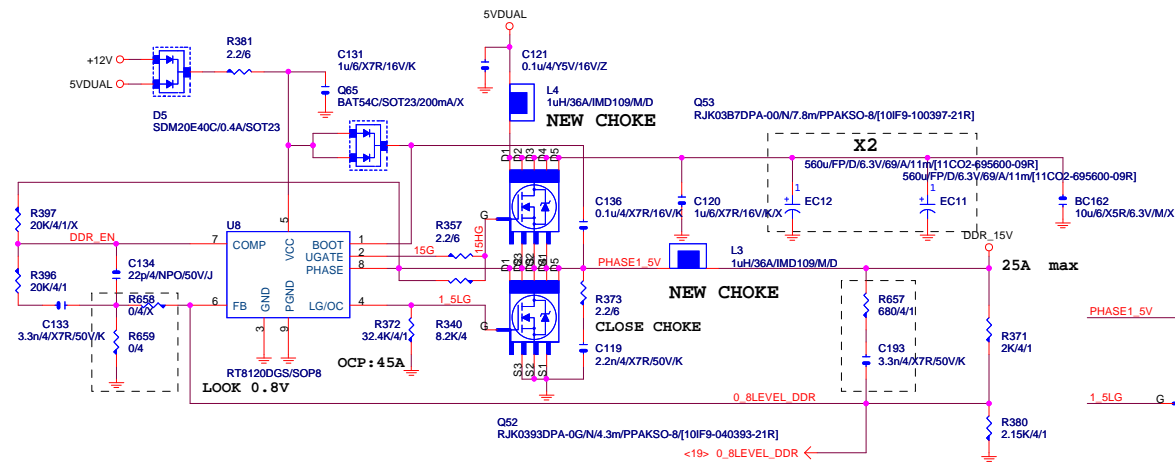


Gigabyte Technology			
Title			
Size			
Document Number			
Date			
Friday, September 13, 2013			
Sheet			
25 of 32			
Rev			
1.11			

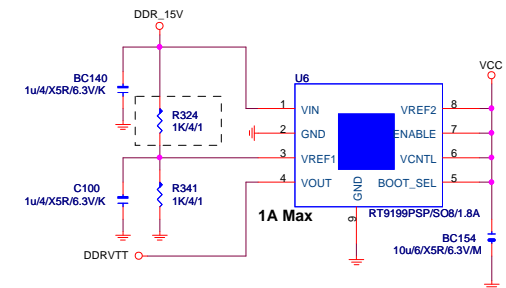




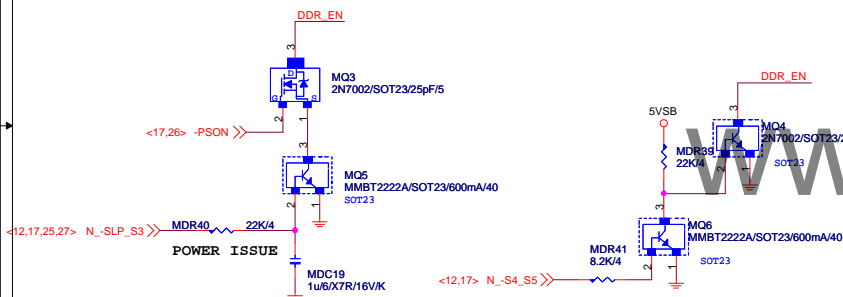
DDR15V



DDRVTT

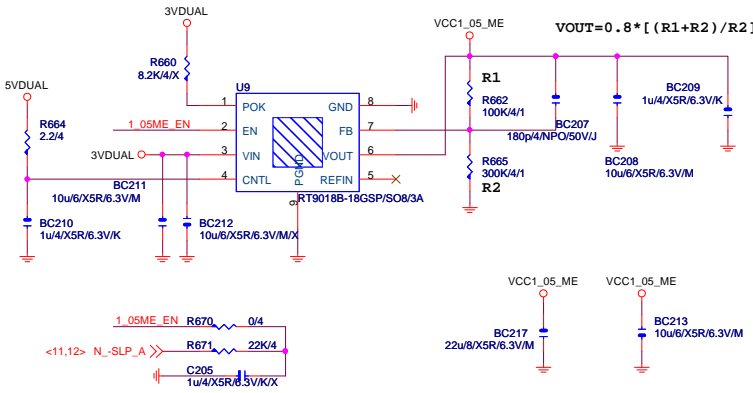


PWR SEQ

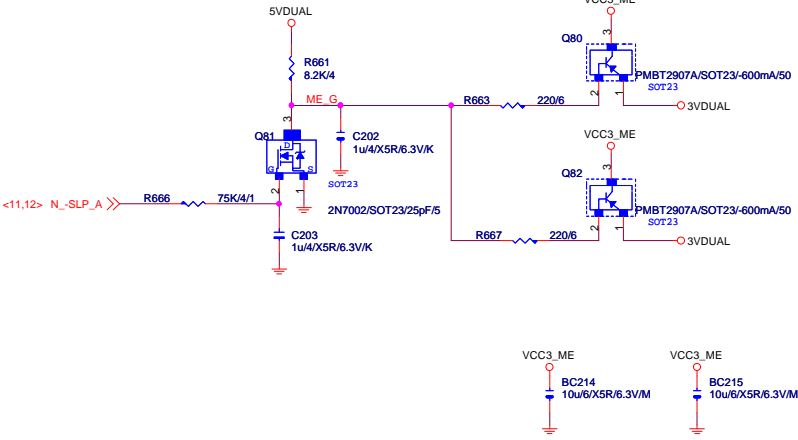


VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1
IRMS=11.45A
560uF/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A
Coefficient=1.7(85°C), 1(105°C)
VIN Ripple current=4.7X1.7=7.99A(85°C)
-->故固態電容須2X7.99=15.98>11.45A
Rocset=(Iccp*Lgate, rdsn)/Iocset
Rocset=(45A*6.7mOhm)/10uA = 30K
Iocset=10uA

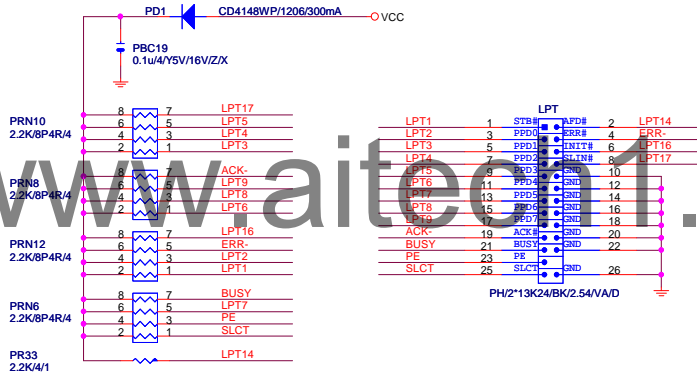
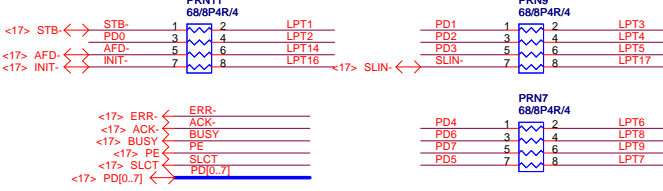
VCC1_05_ME



VCC3_ME



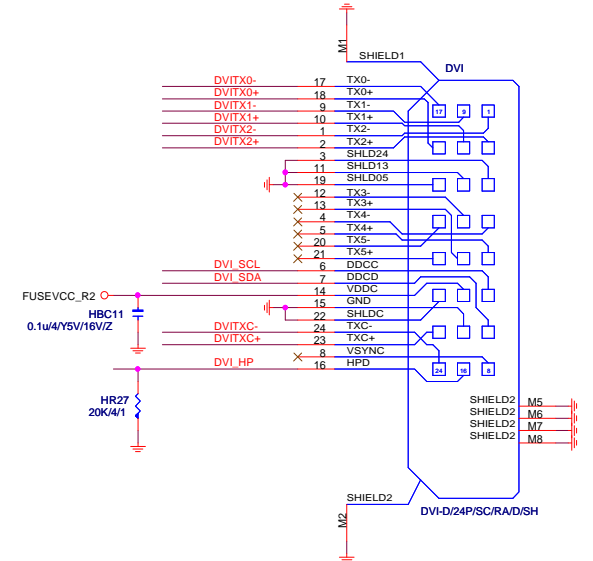
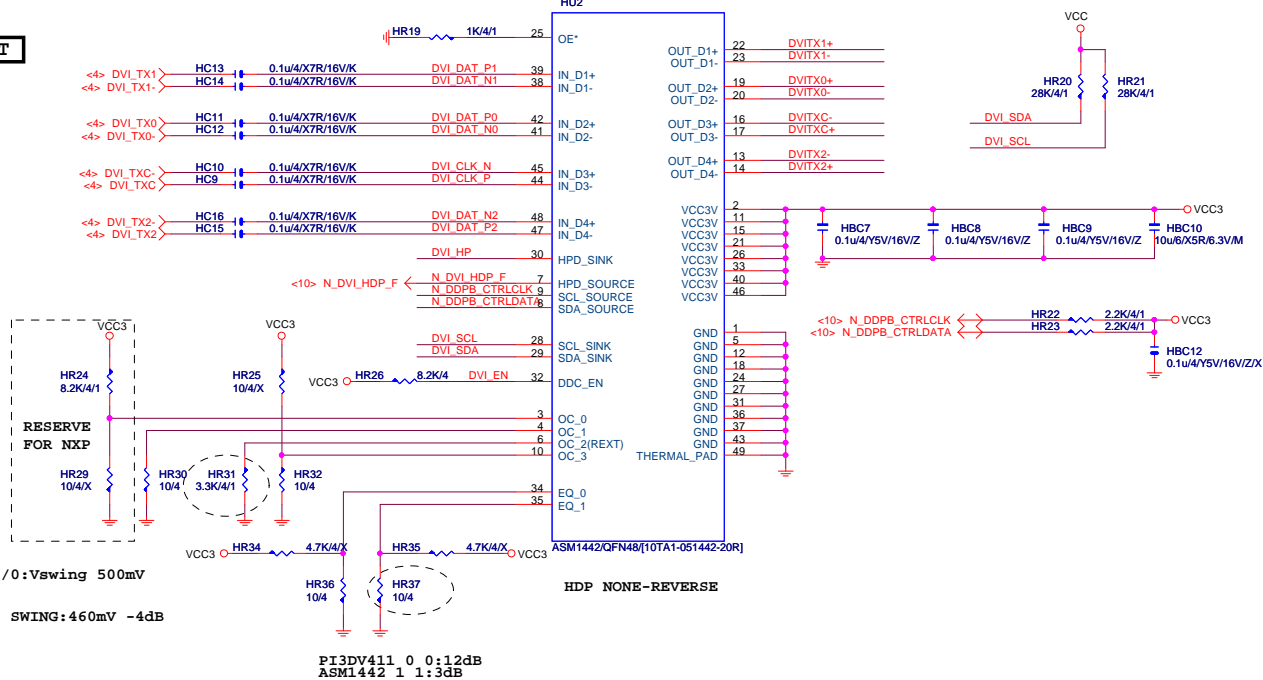
LPT PORT



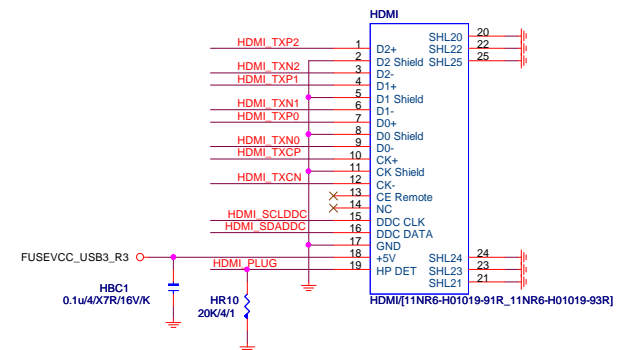
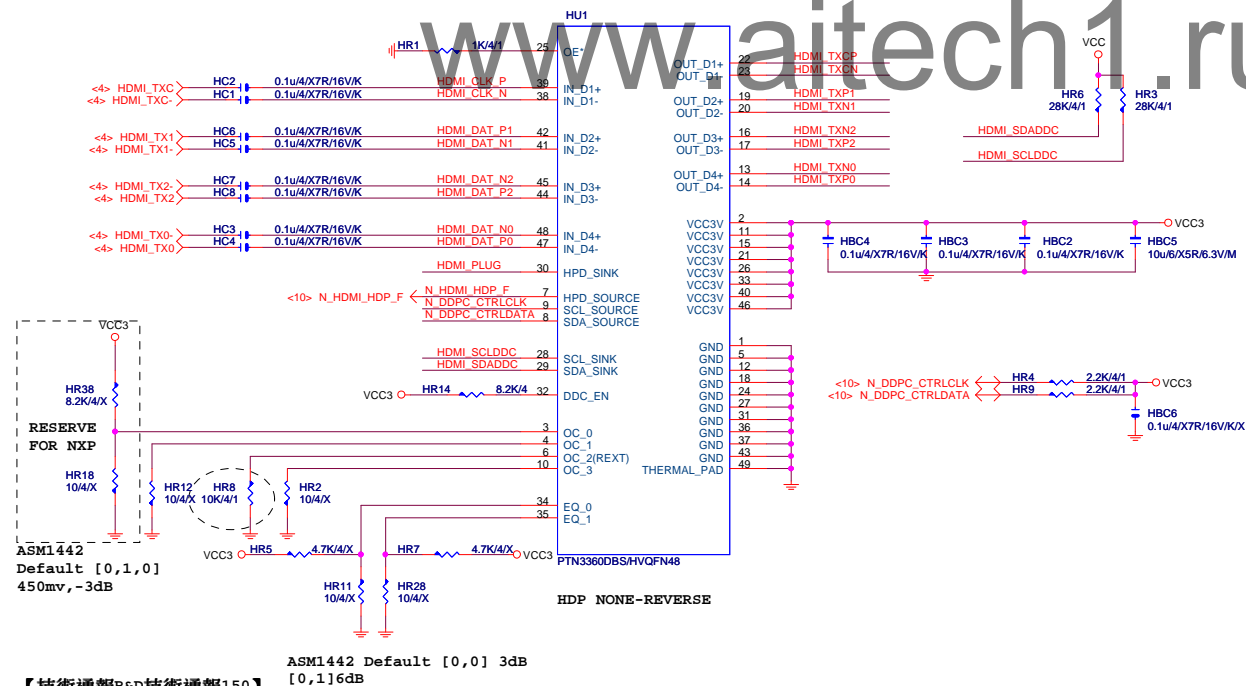
Gigabyte Technology

Title			LPT
Document Number			GA-B85M-D3H
Date			Friday, September 13, 2013
Sheet			30 of 32
Rev			1.11

DVI LEVEL SHIFT



HDMI LEVEL SHIFT



【技術通報R&D技術通報150】

HDMI eye diagram1.4版(deep color)會fail

原因：因目前的HDMI訊號過長，造成RISING TIME過慢，而會壓到eye diagram

改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

PCIE TO PCI

PCI:5/4/5 Impedance=50 +- 15%

BA_D[0..31] <-> BA_D[0..31] <16>

BC_BE0 <-> BC_BE0 <16>
BC_BE1 <-> BC_BE1 <16>
BC_BE2 <-> BC_BE2 <16>
BC_BE3 <-> BC_BE3 <16>

BPERR <-> BPERR <16>
BSERR <-> BSERR <16>

BPAR <-> BPAR <16>
BPLOCK <-> BPLOCK <16>
BDEVSEL <-> BDEVSEL <16>
BSTOP <-> BSTOP <16>
BTRDY <-> BTRDY <16>
BIRDY <-> BIRDY <16>
BFRAME <-> BFRAME <16>

PCIE_RST <-> PCIE_RST <14,15,17>

BPCIRST <-> BPCIRST <16>

BREQ0 <-> BREQ0 <16>
BREQ1 <-> BREQ1 <16>
BGNT0 <-> BGNT0 <16>
BGNT1 <-> BGNT1 <16>

BPCIPME1 <-> BPCIPME1 <16>



High: Enable PCI CLK 66MHz
Low: Disable PCI CLK 66MHz



High: PCICLK INPUT form CLK Gen
Low: PCICLK OUTPUT form IT8893 chip

Co-Lay IT8893 (IT8893 CLKOUT1 N/A)

IT8892: PR24 -> 47ohm
IT8893: PR24 -> 22ohm

IT8892: PR46 -> X
IT8893: PR46 -> O

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

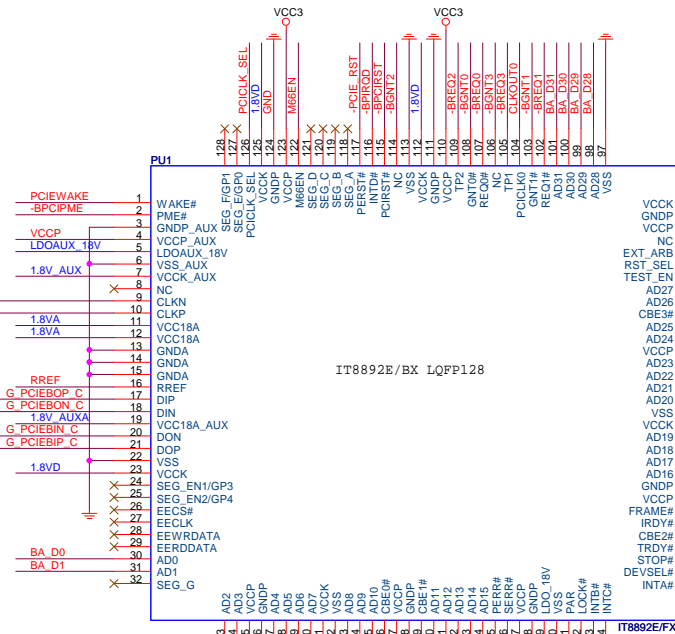
IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X

IT8892: PR19 -> O
IT8893: PR19 -> X



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IT8892 PCI slot

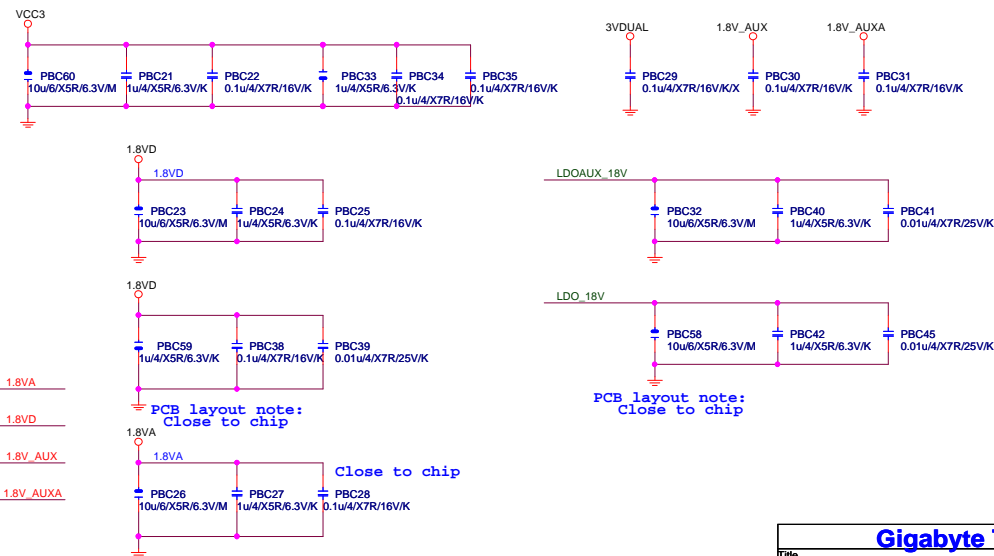
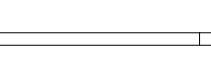
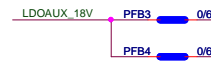
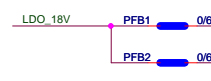
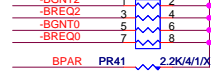
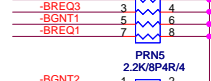
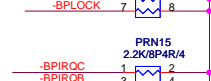


PCI slot



chipset side

3VDUAL



PCB layout note:
Close to chip

PCB layout note:
close to chip

Gigabyte Technology

Title			ITE IT8892E
Size			GA-B85M-D3H
Document Number			Rev 1.1
Date			Friday, September 13, 2013
Sheet			32 of 32